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# Parallel Programming and Heterogeneous Computing

A2 - Parallel Hardware

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## Types of Parallel Hardware



#### **Task Level Parallelism**

Multiple operations are executed in parallel.

## Data Level Parallelism

The same operation is applied in parallel to multiple units of data.





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# Hardware Taxonomy [Flynn1966]





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Chart 3

# Hardware Taxonomy [Flynn1966]







**Multiple** 

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Chart 4

## MISD Hardware

Most exotic class of parallel hardware, not in mainstream use.

- Redundant systems like safety-critical embedded controllers or high-reliability mainframes
- Parallelism not for performance, but dependability



Example: Triple Modular Redundant Architecture

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#### Not covered in this lecture.

#### **Covered in chapter C.**

## SIMD Hardware

Popular class of parallel hardware for special purpose systems.

- = Vector processors
- Early examples: ILLIAC IV, Cray-1, ...

Recently in widespread use:

- GPUs
- Instruction Set Extensions (AltiVec, SSE, AVX, ...)

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Chart **6** 



NVidia Pascal GPU Module







## **MIMD** Hardware

Classic and most general class of parallel hardware.

Wide range of systems from = Multicore CPUs to Supercomputers and Clusters

POWER9 Die with 24 Cores

Variety of architectures and characteristics requires further distinction



Summit Supercomputer



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## MIMD Hardware Taxonomy





## MIMD Hardware Taxonomy



**Parallel Hardware** Lukas Wenzel Multiprocessor Multicomputer VS. Chart 9 see [Tanenbaum1985], [Foster1995], [Pfister1998]

HP

Hasso Plattner

Institut



Processing elements can directly access a **common address space** 

#### Uniform memory access (UMA) system

Processing elements observe the same memory access characteristics over the entire memory.

Simple to program against, but scalability issues

#### Non-uniform memory access (NUMA) system

Processing elements have different access characteristics for different memory regions

> Scales well, but unaware programs can exhibit performance issues

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## SM-MIMD Hardware





#### Processing elements can access their **private address spaces** and **exchange messages**

**Cluster**: Multiple independent machines connected through a network

- **Compute** cluster: Speedup
- **Load Balancing** cluster: Throughput
- High Availability cluster: Dependability

All clusters are distributed systems, but only compute clusters intended for parallel workloads.

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This lecture considers only compute clusters.

## DM-MIMD Hardware

#### Simple way of scaling available compute resources:

Just connect multiple machines in a network.

#### **Dominant architecture for High-End Systems:**

Especially High-Performance Computing

- 1995 *Toy Story* Render Farm 117 nodes × 2 CPUs = 234 CPUs
- 2001 *Monsters Inc.* Render Farm 250 nodes × 14 CPUs = 3500 CPUs
- 2019 Summit cluster (TOP500 #1 in 2019) 4608 nodes, 2 PB RAM, 10 MW power × 2 CPUs × 22 Cores = 202 752 Cores × 6 GPUs = 27 648 GPUs

Summit Cluster

Cluster of RaspberryPI Singleboard Computers



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#### Chart 13



Computers





Literature



## [Flynn1966]

"Very High-Speed Computing Systems" Flynn, Michael J. Proceedings of the IEEE 54.12 (1966) IEEE

## [Tanenbaum 1985]

"Distributed Operating Systems" Tanenbaum, Andrew S and Van Renesse, Robbert. ACM Computing Surveys 17.4 (1985) ACM

## [Foster1995]

"Designing and Building Parallel Programs" Foster, Ian (1995) Addison-Wesley

## [Pfister1998]

"In Search of Clusters" Pfister, Gregory F. 2nd edition (1998) Prentice-Hall Inc

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Chart 14



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# And now for a break and a bowl of Sencha.